**CURRICULUM VITAE**

**Name: BASA.RAKESH M: 9705537609**

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CAREER OBJECTIVE:

Aspiring for a challenging and growth oriented career in any of the professional organization, where I can use and develop my skills and contribute to the progress of the organization.

KEY STRENGTHS:

* Great passion to learn.
* Enthusiastic and patient to achieve the assigned work.
* Efficient interpersonal ability and team player capability.
* Confident in my efforts and planned work

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| **CLASS/DEGREE** | **BOARD/UNIVERSITY** | **INSTITUTION**  **STUDIED** | **YEAR OF PASSING** | **PERCENTAGE** |
| B-TECH | JNTU-H  (Hyderabad) | JYOTISHMATHI COLLEGE OF ENGINEERING  (JCET) | 2015 | 68.17% |
| INTERMEDIATE | ANDHRA PRADESH  STATE BOARD | ARYABHATTA JUNIOR  COLLEGE | 2011 | 80% |
| SSc | ANDHRA PRADESH  STATE BOARD | ZPHS. SCHOOL | 2009 | 81% |

ACADEMIC CREDENTIAL:

SKILL SET:

* **LANGUAGES known           :** Verilog design and verification, system verilog verification
* **:Universal Verification Methodology**

IT EXPOSURE:

|  |  |
| --- | --- |
| Operating system | Linux |
| Other Packages | MS-Word, Excel,  MS PowerPoint |

PROJECT WORK:

"Implemented a major project called **fast addition of two numbers** by using **quaternary signed digit** (**QSD**) numbering system.(B-tech)"

**QSD:** With the binary number system, the computation speed is limited by formation and propagation of carry especially as the number of bits increases. Using a quaternary Signed Digit number system one may perform carry free addition, borrow free subtraction and multiplication. A carry free arithmetic operation can be achieved using a higher radix number system such as Quaternary Signed Digit (QSD). In QSD, each digit can be represented by a number from -3 to 3. Carry free addition and other operations on a large number of digits such as 64, 128, or more can be implemented with constant delay and less complexity. Design is simulated & synthesized using Modelsim6.0.

**“**ROUTER1X3**”**

In this project I had not made Router I has just analysed the working of router. In this project we were had 1 Input line and 3 Output line . The data were send in the form of Header,Payload,Parity we were checking that at output exact data is coming or not or data is being corrupted. I had use Verilog for complete analysing of the Router.

PERSONAL PROFILE:

**Full Name : RAKESH.BASA**

**Father’s Name : PRAKASH.B**

**Mother’s Name :** MADHAVI.B

**Date of Birth**  **:12 AUG 1994**

**Gender :** Male

**Languages Known :** ENGLISH,HINDI,TELUGU

**Marital Status :** Single

**Residential Address : H.no:7-100,Jangampally,kamareddy**

Telangana ,pin code:503102

**Hobbies :** Tennis,Reading Books.

**Declaration:**

I hereby declare that all the information and facts furnished above are true to the best of my knowledge and belief.

Date:

Place: Bengaluru

**(RAKESH.BASA)**